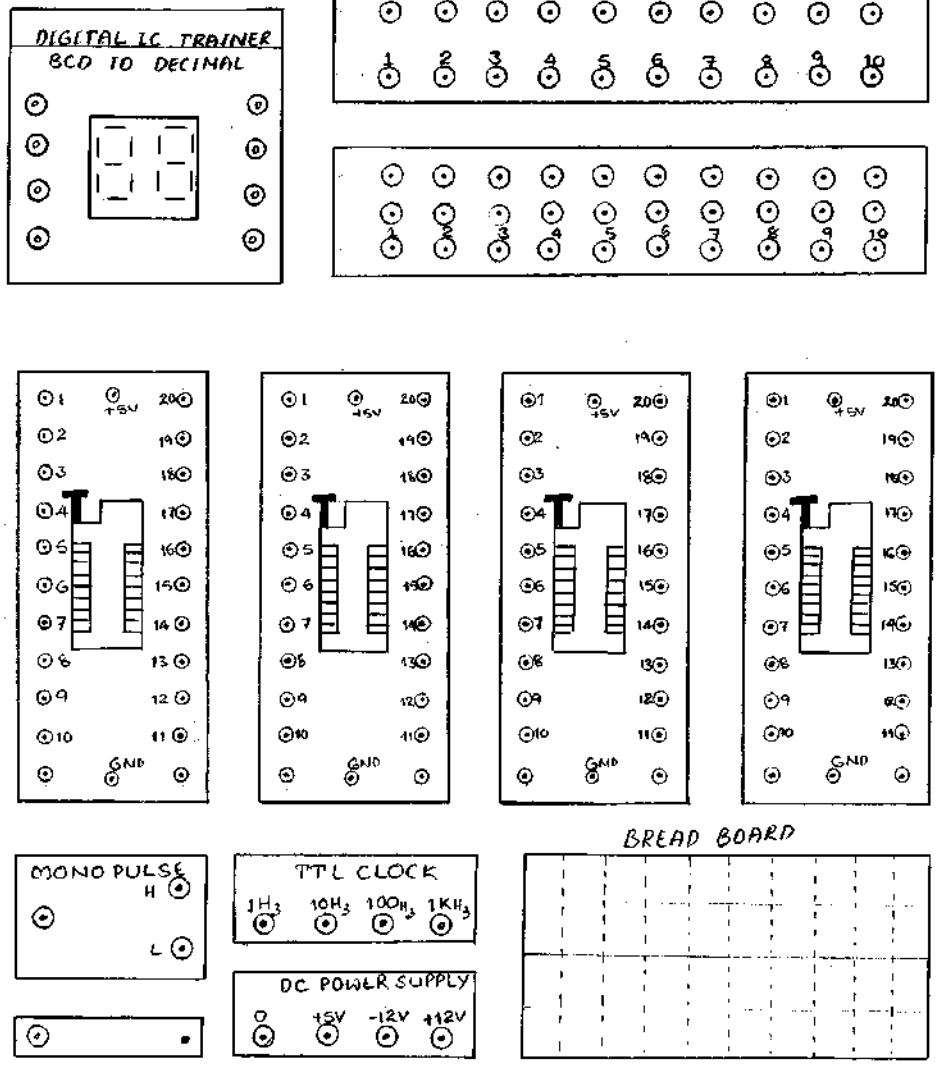
DIGITAL IC TRAINER



Date

Expt. No. 1 Page No. 1

Experiment - 1: Familiarization of Digital Trainer kit, IC Tester, Logic Probe.

Digital Trainer Kit: It is an instrument which is used to conduct the digital experiment. It consists of IC sockets, Logical inputs, Logical outputs, clock signals & supply. The LED's are used to indicate the logic states. In some kits RED for HIGH & GREEN for LOW (0). But in some other kits, ON for High (1) & OFF for low (0). which uses single colour LED. The trainer kit consists of ZIF (Zero Insertion Force) sockets to insert the IC's. The connecting wires used to connect b/w the IC's are called "Patch chords". This patch chords can be shorted for more connections of some signals. If more logical input are required in any circuit, then ground & vcc can be used for input. If IC socket is bigger than IC, the IC is inserted from the top of the socket for easy pin counting.

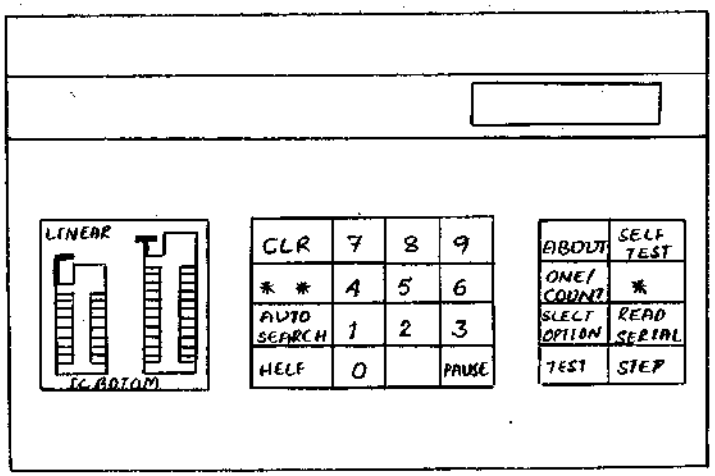
For sequential circuits like counters, shift resistors etc. clock is used generally all types of kits consists of 1Hz to 1KHz range clock. The 1Hz clock is most popularly used for studying. The monopulse is used to give single pulse for the circuit by pressing push button. Some kits consist of bread board for complex circuit connections. The digital trainer kit different from model & manufacturer.

Ic Tester:

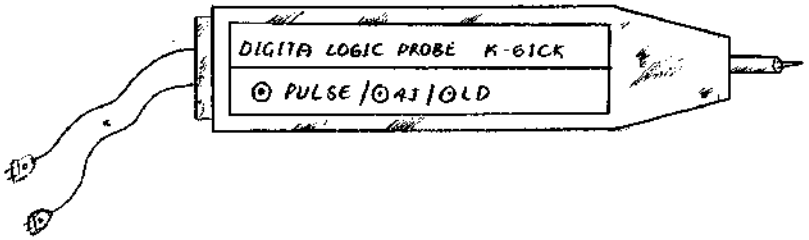
It is a testing instrument which is used to test the IC's good or bad. It consists of ZIF socket, keypad LED & LCD Display. The IC is inserted in the socket & IC number is entered after testing, its display good or bad some IC

Teacher's Signature : _____

IC TESTER



LOGIC PROBE



Date

Expt. No. Page No. 2

Testers consists of auto tests & search function to test & to identify unknown IC.

There are 2 types of IC testers

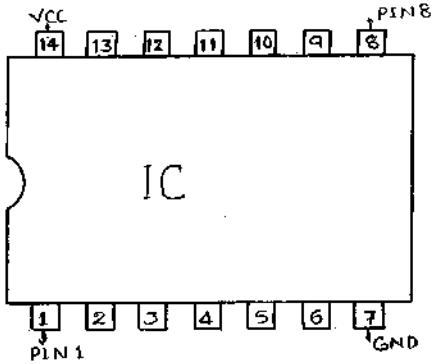
i) Digital IC Testers: It is capable of testing only digital IC's like gates, flip flops, shift registers, counters etc.

ii) Analog IC Testers: It is capable of testing only analog IC's like timers, OP amplifiers, regulators, drives circuit etc.

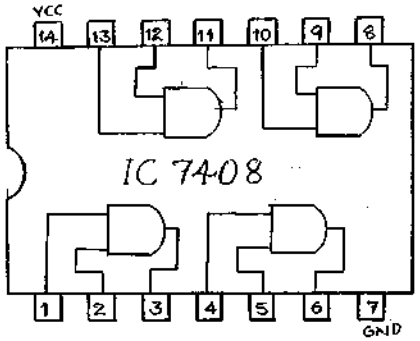
Logic Probe:

It is a testing instrument that is used to check the logic states in digital circuits. It consists of "TIP" to place IC pins & 3 different colours LED's to indicate logic state. The power is connected from the test circuit. The toggle switch used to select between TTL & CMOS logic level testing. The logic states indication is as follows.

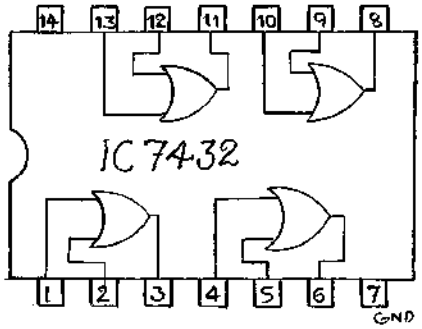
Teacher's Signature :



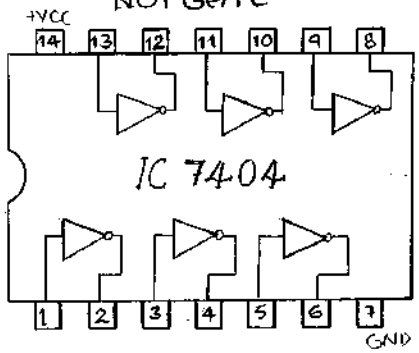
AND GATE



OR GATE



NOT GATE



Date .....

Expt. No. 2 Page No. 3

Experiment - 2

Study of IC MANUAL & FAMILIARISATION OF IC & IC's Families.

An IC is an electronic integrated circuits moulded on sc chip. The IC is small so all the electronic instrume-nts like TV, computer etc are small in size.

The IC are of 3 types. They are;

i) Digital IC: Gates, flip-flops, counters, shift registers, memory.

ii) Analog IC: Timers, pumps, regulators, Drivers.

iii) High Level IC; Micro controllers, micro processor (ADR)

IC's are manufactured in different package but DIP (dual inland package) is most popular IC package.

On top of each IC chip, the following information is usually printed.

1. Manufacturers name, symbol or initial,
2. The manufacturer year & week or Data code.
3. The 7400 series number of the chip, the different technology used to design the circuit inside the IC, some of populas IC technology are;

i) Transistor To Transistor Logic (TTL)

ii) Emmiter coupled logic (ECL)

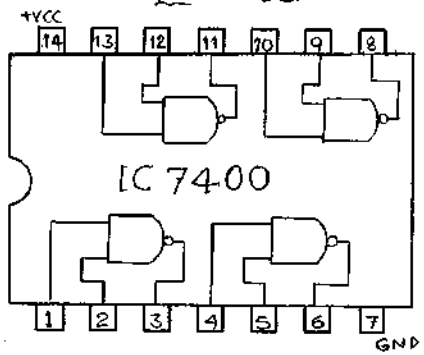
iii) CMOS Logic

iv) PMOS Logic

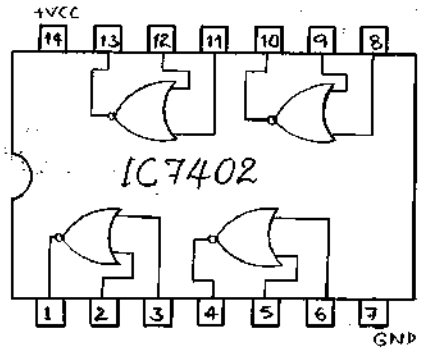
v) NMOS logic

Teacher's Signature : _____

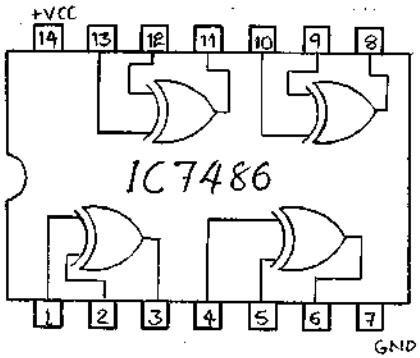
NAND GATE



NOR GATE



X-OR GATE



Date .....

Expt. No. .....

Page No. 4

The TTL logic family is most widely used logic family This is again divided into categories. Some of the categories are follows.

CATEGORY	PREFIX	EXAMPLES	USER
Standard TTL	74	7400, 7447	GENERAL
High power TTL	74H	74H00, 74H77	High power
Low power TTL	74L	74L00, 74L47	Low power
Schottkey TTL	74S	74S00, 74S47	High Speed

The logic circuits of different families are fabricationed on IC by using any one of the following integration technology

i) SSI ; Small Scale integration - It allows upto 12 gates per IC.

ii) MSI : Medium Scale integration : It allows 12/99 gates per IC

iii) LSI : Large Scale integration - It allows 100 to 999 gates per IC

iv) VLSI ; Very Large Scale integration - It allows 1000 or more gates/IC.

Terminology used in Books.

i) '0' - Low level
ii) '1' - High level
iii) 'Z' - Open State
iv) 'x' - Don't care condition.
v) '↑' - Raising clock or High going clock
vi) '↓' - Falling clock or Low going clock

Teacher's Signature : _____

Date .....

Expt. No.....

Page No....5.....

Familiarisation of IC;

Ic Number	Ic Description
7432	Quadrilateral 2 input OR Gate
7408	Quadrilateral 2 input AND GATE
7404	Miscellaneous Inverter
7486	Quadrilateral Exclusive OR GATE
7400	Quadrilateral 2 input NAND GATE
7402	Quadrilateral 2 input NOR GATE
7410	Triple 3 input NAND GATE
7474	Dual D-type Flop
7476	Dual JK Flip Flop
74373	Octal transparent latch
74374	Octal flip-flop
7483	4 bit Adder
7485	4 bit Substracter
7447	BCD to 7 Segment decoder
74138	1:8 de multi processor.
74151	8:1 Multiplexer.
74147	Decimal to binary priority
74153	Dual 4:1 Multiplexer

The 5400 series are used for military applications with temparature rating of 55°c to 125°c & 7400 series are used for commercial applications with the temperation of digital Ic as given by manufacturer.

1) Vcc; The Ic supply voltage to be converted b/w Vcc & ground terminal for normal.

Teacher's Signature : _____

Date .....

Expt. No.....

ii) TA ; Operating free air temperature.

iii) VIH: High level input, voltage, their is the minimum input voltage which is recognised by the logic gate.

iv) VIL ; Low level input voltage their is the minimum voltage which is recognised by the gate as logic gate.

v) VOH; Low level output voltage This is the minimum voltage available at the output corresponding to logic gate

vi) IIH; High level input current, this is the minimum current which must be supplied by driving a source correspondin-g to first level.

vii) VOL; Low level input voltage, this is the minimum voltage avail-able at the output corresponding to logicals.

viii) IIC; Low level input current, this is the maximum current which much be supplied by a driving source corresponding to zero level voltage.

ix) IOH; High level output current, this the maximum current which the gate can sink on level.

x) IOL ; Low level output current, this is the maximum current which the gate can sink '0' level.

xi) tPLH or tPHL (Turn on propogation delay); This is the '0' time when output goes from logic ONE to logic 0 level. This is also called as "Falling time".

xii) tPHL ; (Turn off propogation delay). This is the delay time when the output goes from logic zero to logic ONE level. This is also refered as the "RAISING TIME".

Teacher's Signature : _____

Date .....

Expt. No.....

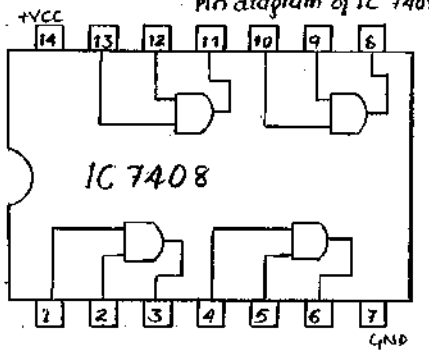
Page No...1.....

Parameter	7400	74A500	Units
V_{IH}	2	2	V
V_{IL}	0.8	0.8	V
V_{OH}	2.4	2.7	V
V_{OL}	0.4	0.5	V
I_{IH}	40	20	mA
I_{OH}	-400	-200	μA
I_{OL}	16.0	8	mA
T_{PHL}	15.0	18	ns
T_{PLH}	22.0	15	ns
I_{IL}	-1.6	-0.36	mA

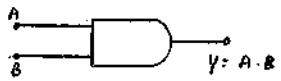
Teacher's Signature : _____

1 AND GATE

Pin diagram of IC 7408



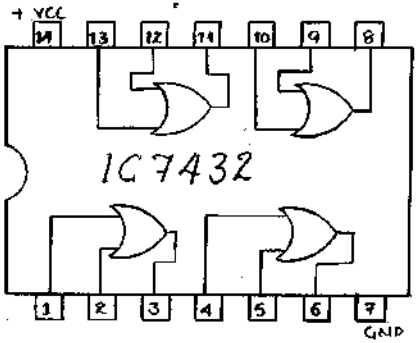
Logic symbol



TRUTH TABLE

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

2. OR GATE

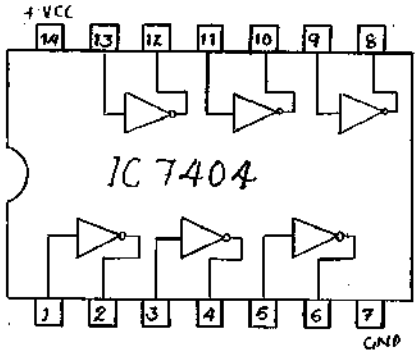


Logic Symbol

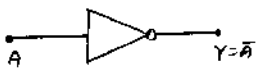
TRUTH TABLE

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT GATE



Logic Symbol



INPUT	OUTPUT
A	Y = Ā
0	1
1	0

Date .....

Expt. No. 01 Page No. 8

Experiment - 1: Verification of logic gates

Aim: Familiarization of gates using 7432, 7408, 7404, 7486, 7400 & 7402

Apparatus: Digital trainer kit, patch chords, Ic 7432, 7408, 7404, 7486, 7400 & 7402.

Theory: A gate is an electronic circuit which consists of one or more inputs & single output. It is basically a building block in digital electron. The gates are classified into 7 types based on their function.

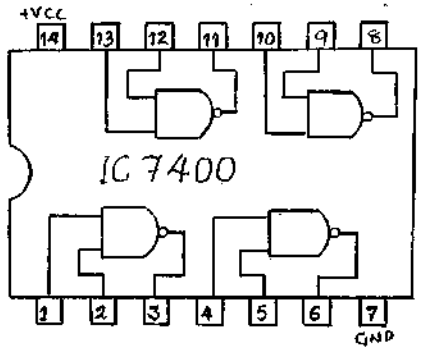
1. AND GATE: It consists of two or more input & only one output. It gives the "HIGH" output when all the inputs are "HIGH". The output is "low" when a one of the input is "Low". The 7408 IC consists of 4 two inputs AND gate. AND gate gives the output which is logical multiplication of the inputs.

2. OR GATE: It consists of 2 or more inputs & only one output. It gives "HIGH" output if any one of the inputs is "HIGH". The output is low when all the inputs. OR gate gives the logic addition of the inputs.

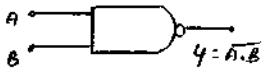
3. NOT GATE: It consist of one input & one output. It gives "HIGH" output for low input & low output. 7404 IC consists of 6 NOT gate. It gives the compliment or inverted output of the input.

Teacher's Signature : _____

4. NAND GATE



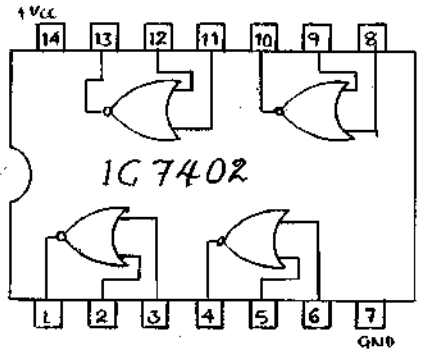
Logic Symbol



TRUTH TABLE

INPUT		OUTPUT
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

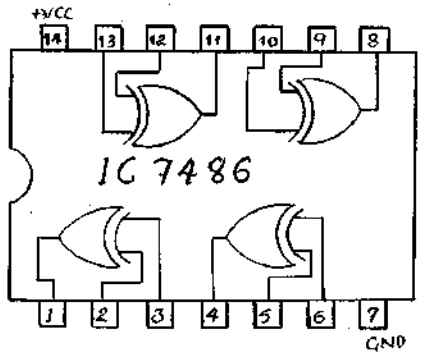
5. NOR GATE

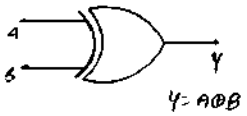


TRUTH TABLE

INPUT		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

6. X-OR GATE





TRUTH TABLE

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Date .....

Expt. No. ..... Page No. ...9...

4. NAND GATE; It consist of 2 or more inputs & only one output. The output is "HIGH" when any one of the input is "Low" and output is low when all the inputs are "HIGH". It gives the inverted output after the logical Multiplication of the input. The 7400 IC consists of 4 two input NAND gates.

5 NOR GATE; It consists of 2 or more inputs & only 1 outputs. Output is "HIGH". When all the input are low & output is low. When any 1 of the input is "HIGH" It gives the inverted output after the logical addition of the inputs. The 7402 IC consists of 4 two input "NOR" gates.

6. X-OR GATE: It consists of 2 or more inputs & 1 output. It gives "HIGH" output, when inputs are not equal & low input when inputs are equal when 7486 IC consists of 4 two input X-OR gate.

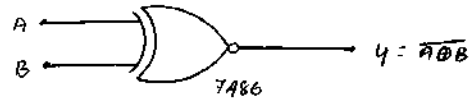
7. X-NOR GATE; It consists of 2 or more inputs & only one output It gives "HIGH" output when inputs are equal & low when inputs are not equal. There is no specific IC for X-NOR gate. It can be constructed by using X-NOR & NOT

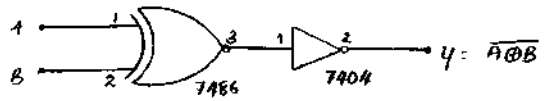
Procedure;

1. Write pin number for all the gates by refering IC PIN number.
2. Insert the required IC in ZIF Socket in proper direction.
3. Connect Vcc & GND terminals for Vcc & Ground

Teacher's Signature : _____

7. X-NOR GATE





TRUTH TABLE

INPUT		OUTPUT
A	B	$Y = \overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

Date .....

Expt. No..... Page No. 10

Sockets in trainer kit.

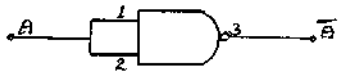
4. Connect the inputs A and B of the gate to the logic gate
5. Connect the output Y to the logical output
6. Verify the truth table by changing input combination and observe the output for input combenation.

RESULT:-

The truth tables of all logic gates are verified and functions are observed.

Teacher's Signature : _____

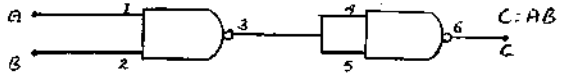
1. NAND AS A NOT GATE



TRUTH TABLE

A	$\overline{A}$
0	1
1	0

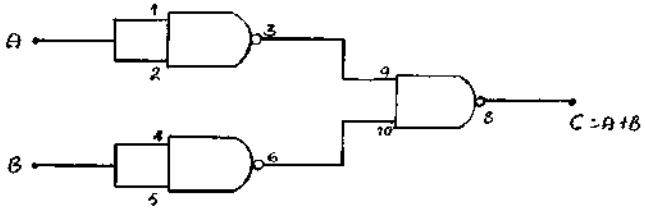
2. AND FROM NAND GATE



TRUTH TABLE

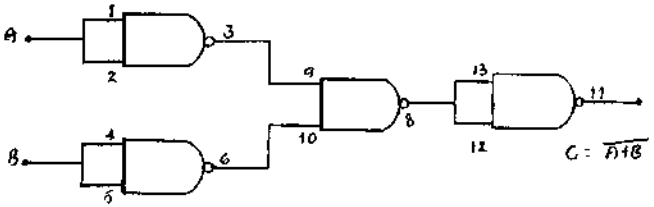
INPUT		OUTPUT
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

3. OR GATE USING A NAND GATE



INPUT		OUTPUT
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

4. NOR GATE USING A NAND GATE



INPUT		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Date .....

Expt. No. 02 Page No. 11

Experiment - 2 : Realization of NAND gate using IC 7400 as a Universal gate

Aim : Realization of NOT, OR, AND, NOR, X-OR and X-NOR using NAND gates

Apparatus : Digital Trainer Kit
Patch cards - 15 NOS
7400 - 2 NOS

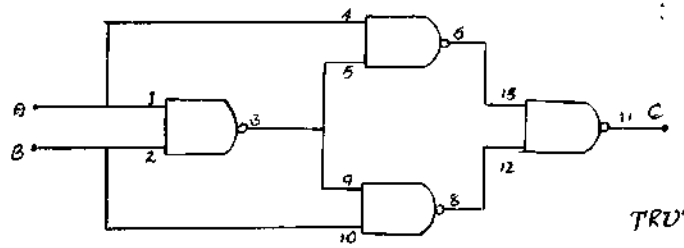
Theory : The NAND gate is a logic gate which gives the inverted output of logical multiplication of two or many inputs. It can be used to construct any logic gate or any logic functional. So it is universal gate.

Procedure :

1. Write logic functions & truth tables
2. Insert the required IC in ZIF SOCKET in proper direction
3. Connect the supply terminals
4. Connect the circuit starting from the input side
5. Connect the output y to the logical output
6. Switch ON the Trainer
7. Verify the truth table by changing the input combination & observe the output for each combination.
8. Repeat steps 2 to 7 for all the gates.
9. Write the result.

Teacher's Signature : _____

5. XOR GATE USING NAND GATE



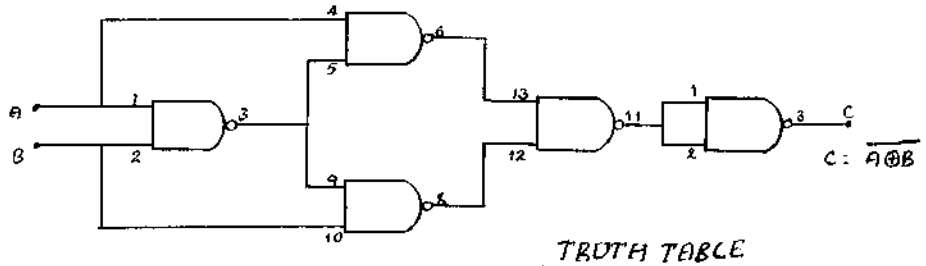
$C = A \oplus B$

$= A.\bar{B} + B\bar{A}$

TRUTH TABLE

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

6. X-NOR GATE USING NAND GATE



$C = \overline{A \oplus B}$

TRUTH TABLE

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

Date .....

Expt. No. .....

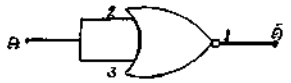
Page No. 18

Result;

All the gates have been verified using NAND gates (IC 7400)

Teacher's Signature : _____

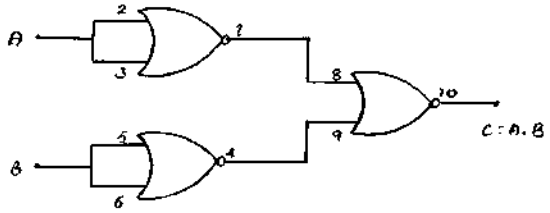
1. NOT GATE USING NOR GATE



TRUTH TABLE

A	$\bar{A}$
0	1
1	0

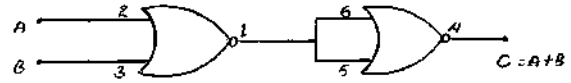
2. AND GATE USING NOR GATE



TRUTH TABLE

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

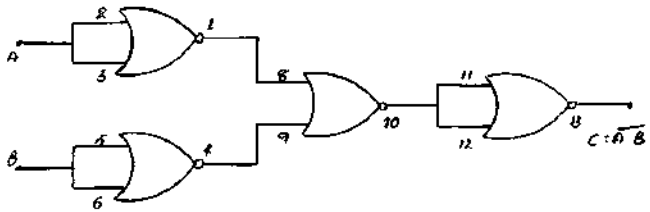
3. OR GATE USING NOR GATE



TRUTH TABLE

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

4. NAND GATE USING NOR GATE



TRUTH TABLE

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Date .....

Expt. No. 05 Page No. 13

Experiment - 3

NOR Gate as an Universal gate using IC 7402.

Aim: Realization of NOT, OR, AND, NAND, XOR & XNOR gates using NOR gate

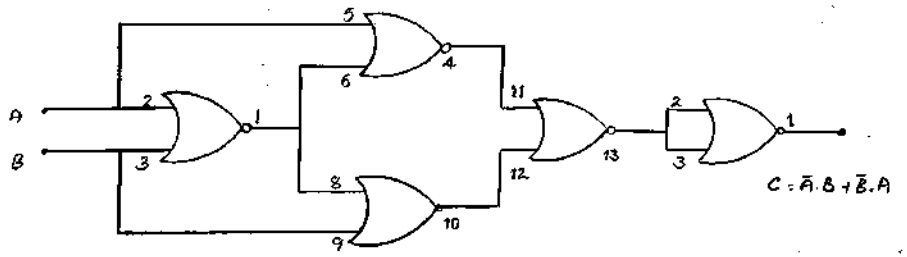
Apparatus: The NOR gate is the logic gate which gives the inverted output of logical addition of two or many inputs. It can be used to construct any logic gate or logic function. So it is called universal gate.

Procedure:

1. Write logic function and truth tables.
2. Insert the required IC in ZIF socket inproper direction.
3. Connect supply terminals
4. Connect the circuit starting from the input side.
5. Connect the output 'Y' to the logical output.
6. Switch ON the Trainer kit.
7. Verify the truth table by changing the input combinations and observe the output for each combination.
8. Repeat steps 2 to 7 for all the gates
9. Write the Results

Teacher's Signature : _____

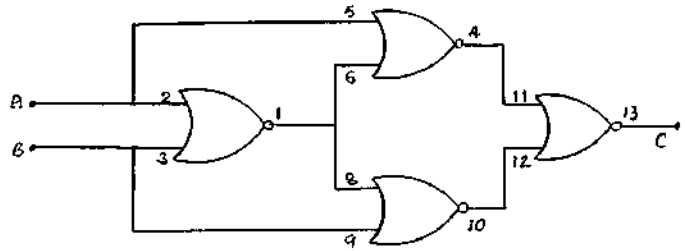
5. X-OR GATE USING NOR GATE



TRUTH TABLE

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

6. X-NOR GATE USING NOR GATE



TRUTH TABLE

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

Date .....

Expt. No. .....

Page No. 14

Result:

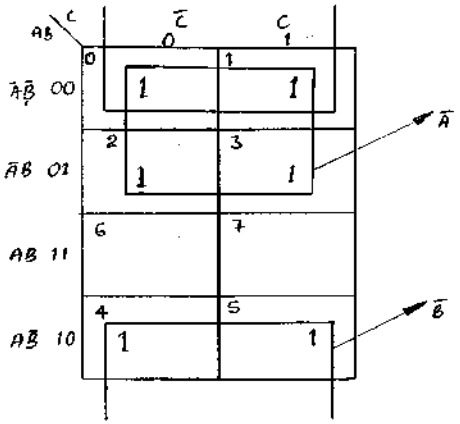
All the gates has been verified using NOR gate IC 7402.

Teacher's Signature : _____

Boolean Expression

$y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + \bar{A}BC + AB\bar{C} + A\bar{B}C$

K - MAP

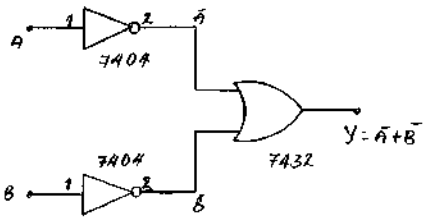


$Y = \bar{A} + \bar{B}$

TRUTH TABLE

A	B	$\bar{A}$	$\bar{B}$	$Y = \bar{A} + \bar{B}$
0	0	1	1	1
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0

Circuit Diagram



Date .....

Expt. No. 04 Page No. 15

Experiment - 04.

Boolean Expression Using K-map.

Aim; Implementation & Verification of Boolean Expression using K-map.

Apparatus; Digital Trainer kit
Patch cards - 2 Nos
7404 - 2 Nos
7432 IC's

Theory;-

The Karnaugh map (K-map) is one of the most popular methods used to reduce the boolean functions. It permits minimisation of expression in a graphic way. The K-map is composed of an arrangement of adjecent cells each representing one particular combination of variables in product form. 1 is placed in cell for each term which leads to a 1 output. Then given Boolean expression can be simplified by grounding the 1s that are in adjacent cells According to the K-map rules.

Procedure;

1. Write a K-map for the given expression.
2. Reduce the Boolean expression by grounding 1s.
3. Write the circuit diagram for reduced Boolean Expression.
4. Connect the circuit.
5. Verify the truth table by changing the input combinations and observe the output for each

Teacher's Signature : _____

Date .....

Expt. No..... Page No. 16.....

Combinations

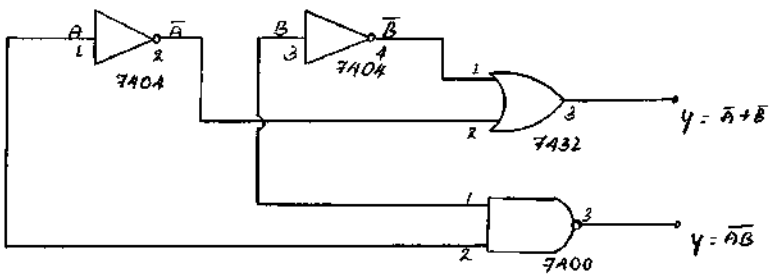
6. Write proper result.

Result :

Boolean expression has been simplified using K-map and its truth table has been verified.

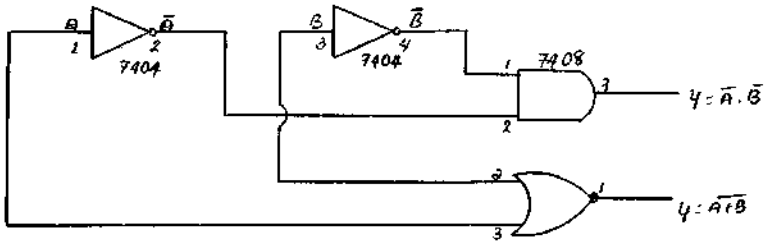
Teacher's Signature : _____

THEOREM : 2



A	B	$\bar{A}$	$\bar{B}$	$\overline{AB}$	$\bar{A}+\bar{B}$
0	0	1	1	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	0	0

THEOREM : 1



A	B	$\bar{A}$	$\bar{B}$	$\overline{A+B}$	$\bar{A}.\bar{B}$
0	0	1	1	1	1
0	1	1	0	0	0
1	0	0	1	0	0
1	1	0	0	0	0

Date .....

Expt. No..... Page No. 17

Experiment - 5

De-morgan's Theorem

Aim: To realize & verify Demorgan's law, & realization of the given expression using de-morgan's Theorem.

Apparatus: Digital Traine kit.
Patch cards - 14 NOS/20 NOS
7404, 7432, 7408, 7400, 7402

Theory: Demorgans theorem are very important theorems in boolean algebra. These are used to reduce the Boolean expression

The first theorem says the "complement of Sum is equal to the product of individual compliments"

$\overline{A+B} = \bar{A}.\bar{B}$

The second theorem says the "compliment of a product is equal to their individual compliments"

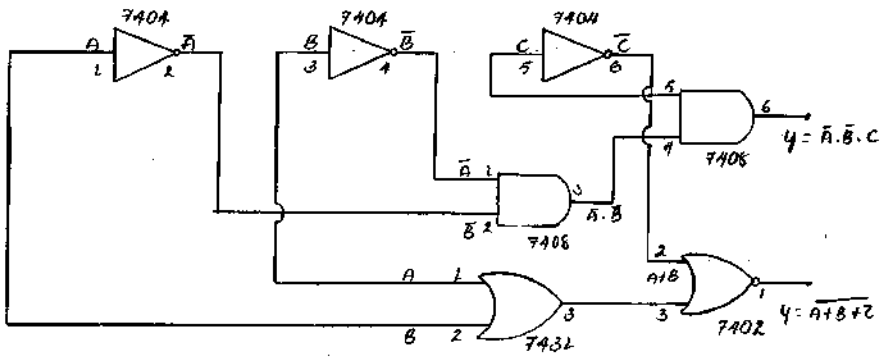
$\overline{A.B} = \bar{A}+\bar{B}$

Procedure:

1. Connect theorem 1 Circuit & verify its truth table
2. Connect theorem 2 Circuit & verify its truth table
3. Convert the given expression into other form
4. Write down the truth table.
5. Connect the circuit as shown in diagram

Teacher's Signature : _____

Boolean Expression:



A	B	C	$\bar{A}$	$\bar{B}$	$\bar{C}$	$\overline{A+B+C}$	$\overline{\bar{A}.\bar{B}.C}$
0	0	0	1	1	1	0	0
0	0	1	1	1	0	1	1
0	1	0	1	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	1	1	0	0
1	0	1	0	1	0	0	0
1	1	0	0	0	1	0	0
1	1	1	0	0	0	0	0

Date _____

Expt. No. _____ Page No. 18

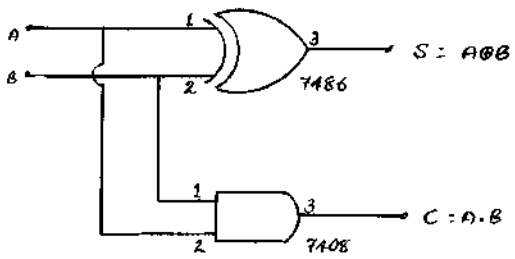
6. Verify the truth table by changing the input combination & observe the output for each combination.
7. Write down the result.

Result;

Demorgans law has been verified. Boolean expression is also verified using IC 7404, 7432, 7402, 7400, & 7408.

Teacher's Signature : _____

HALF ADDER:



TRUTH TABLE

INPUT		OUTPUT	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Date .....

Expt. No. ..... Page No. ..19.....

Experiment - 6

Implementing Half adder & Full adder using logic gates.

Aim; Implementing half adder and full adder using logic gates.

Apparatus; Digital Trainer Kit
Patch cards - 10/18 Nos
7486, 7408 & 7432 IC's.

Theory;

Half Adder; It is a combinational logic circuit whose function is to add 2 binary digits of 1 bit size, producing a sum & carry according to the binary addition.

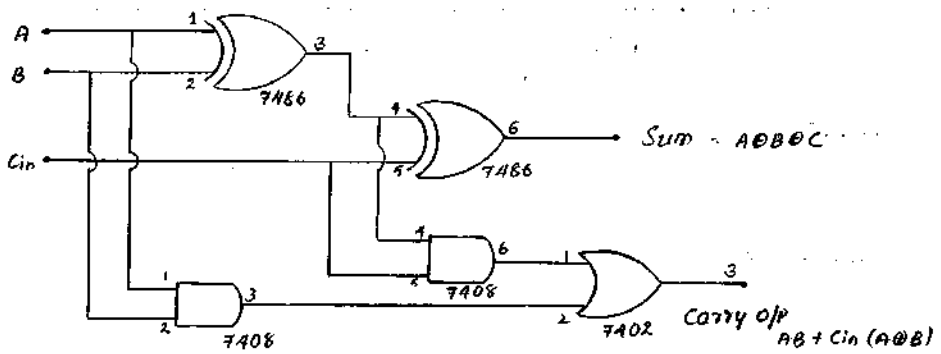
Full Adder; It is a combinational logic circuit with 3 inputs and 2 outputs It adds 2 numbers of 1 Bit size along with carry input It gives the sum & carry as outputs.

Procedure;

1. Write the logic functions & Truth tables.
2. Insert the required IC in ZIF socket in proper direction.
3. Connect the supply terminals
4. Connect the circuit starting from the input side
5. Connect the output y to sum & carry output.
6. Switch 'ON' the function.

Teacher's Signature : _____

FULL ADDER



TRUTH TABLE

INPUT			OUTPUT	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Date .....

Expt. No. ..... Page No. 20

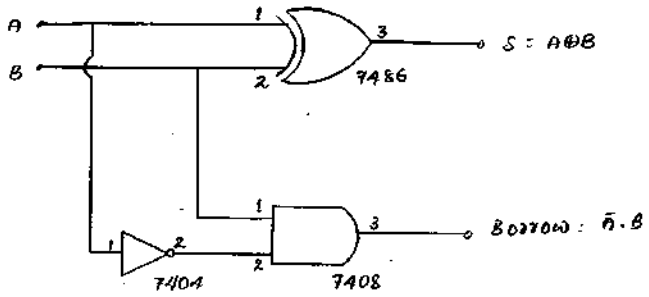
7. Verify the truth table by changing the input combinations & verify the output for each combinations.
8. Write proper conclusion.

Result ;

Half adder and full adder and its truth table has been verified.

Teacher's Signature : _____

HALF SUBTRACTOR



TRUTH TABLE

A	B	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Date .....

Expt. No. ..... Page No. 21

Experiment - 7.

Half subtractor and full subtractor.

Aim; Implementing Half subtractor & full subtractor using logic gates.

Apparatus; Digital Trainer Kit
Patch cards - 13/22 Nos
IC 7486, 7408, 7432, 7404.

Theory;

Half Subtractor; It is a combinational logic circuit whose function is to subtract two binary digits of 1 bit size, producing a difference & a borrow according to binary subtraction rules.

Full Subtractor; It is a combinational logic circuit with 3 inputs & 2 outputs. It subtracts 2 numbers of one bit size along with borrow input. It gives the difference & borrow as outputs.

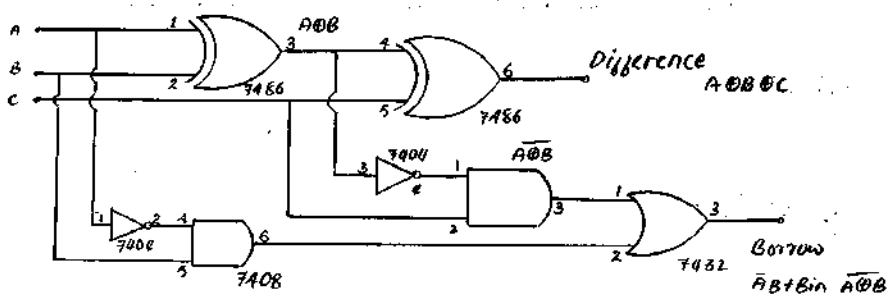
Procedure;

1. Connect Half subtractor circuit and verify its truth table

2. Connect full subtractor circuit and verify its truth table.

Teacher's Signature : _____

FULL SUBTRACTOR;



TROTH TABLE

INPUT			OUTPUT	
A	B	Bin	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Date .....

Expt. No. .....

Page No. 22

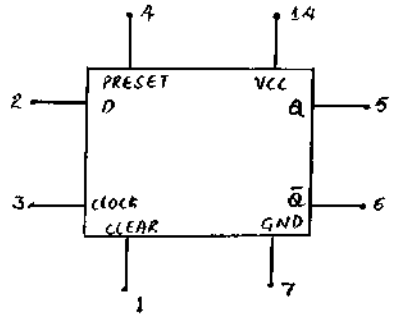
3 Write the proper conclusion.

Result:

Half subtractor and full subtractor and its truth table has been verified.

Teacher's Signature : _____

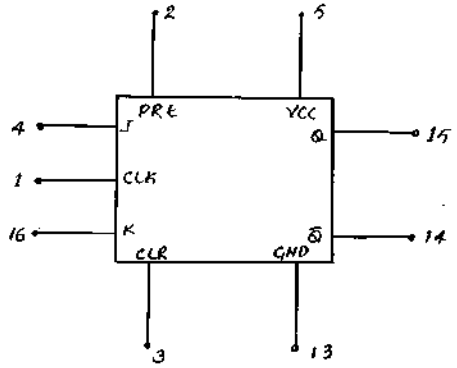
1. IC 7474:



TRUTH TABLE

CLEAR	PRESET	CLOCK	D	Q $\bar{Q}$	OPERATION
0	0	X	X	1 1	INVALID
0	1	X	X	0 1	CLEAR
1	0	X	X	1 0	PRESET
1	1	0	0	Q $\bar{Q}$	LATCH
1	1	1	0	0 1	LOW
1	1	1	1	1 0	HIGH

2. IC 7476.



Date .....

Expt. No. ..... Page No. ...03.....

Experiment - 8

Verification of flip-flops

Aim: Verification of truth table of flip-flop using ICs 7474, 7476, 74373, 74374.

Apparatus: Digital trainer kit.
Patch cards - 09 Nos
7474, 7476, 74373, 74374.

Theory:

What is flop-flop?

The flip-flop is a sequential logic network & bistable multi-vibrator. It can stable in any logic level It is 1 Bit storage device. The flip flop is also basic building block in digital electronics along with logic gates. They are used in different application like counters, shift registors, memory device, latches and etc.

1) 7474:

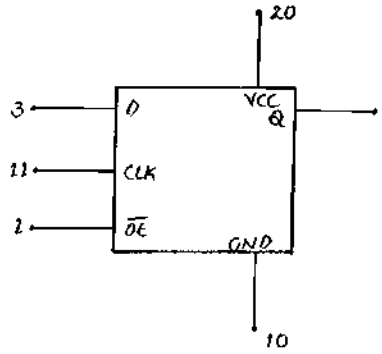
This is consists dual +ve edge triggered 'D' flip-flip is most popular flip-flop. The 'D' flip-flop consists 1 i/p along with clock & 1 or 2 outputs with optional present & clear signals are used to set (store 1) or Reset (store '0') the flip-flop. The 'D' input along with clock is used to store the data into F/F. The output are affected by

Teacher's Signature : _____

TRUTH TABLE

CLEAR	PRESET	CLOCK	J	K	Q	$\overline{Q}$	OPERATION
0	0	X	X	X	1	1	INVALID
0	1	X	X	X	0	1	CLEAR
1	0	X	X	X	1	0	PRESET
1	1	1	0	0	Q	$\overline{Q}$	LATCH
1	1	1	0	1	0	1	LOW
1	1	1	1	0	1	0	HIGH
1	1	1	1	1	INVALID		

3. IC 74373



TRUTH TABLE

$\overline{OE}$	CLK	D	Q	OPERATION
0	1	0	0	LOW
0	1	1	1	HIGH
0	0	X	Q	LATCH
1	X	X	Z	OPEN

Date .....

Expt. No..... Page No...24.....

2) 7476 ; This Ic consists dual -ve edge triggered Jk flip-flops The Jk flip-flop consists 2 inputs J & k. The 'J' is used to set the flip-flop & 'K' is used to reset the flip-flop on -ve edge of clock.

3) 74373 ;

This is octal transperent latch. This Ic consists 8 +ve level triggered 'D' flip-flops with common clock & output enable signal. when output enable signal is low & clock is high 'D' input is transpered to 'Q' output on falling edge of clock data is latched into when clock is zero Q is not depended on D input. It is used for adders demultiplexing in microprocessor applications.

4) 74374 ;

This is octal +ve edge triggered latch. This Ic 8+ve edge triggered D flip-flop with common clock & output enable signal. when output enable signal is low & on raising clock D input is transfered to Q output on high level of clock data is latched into Q. when Q output on high level of clock data is latched into Q. when clock is low or high Q is depended on D input.

Procedure :

1. Connect 7477 signals & verify the truth table
2. Use insert monopulse or its pulse train for clock
3. Connect 7476 signals & verify the truth table
4. Connect 74373 signals & verify the truth table, use

Teacher's Signature : _____

Date .....

Expt. No. ..... Page No. 05

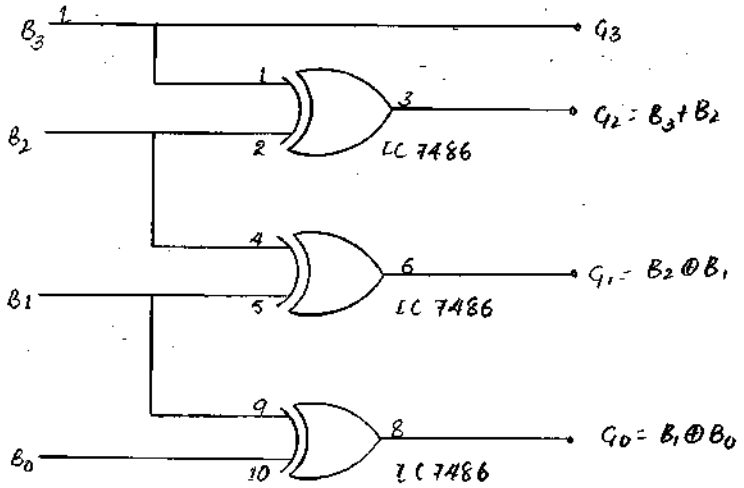
logic input for clock.
5. Check for all 8 flip-flops simultaneously.
6. Connect 74378 signals & verify the truth table. Use input for clock
7. Write proper result

Result:

The truth tables of flip-flops using IC 7474, 7476, 74373 & 74374 has been verified.

Teacher's Signature : _____

Circuit Diagram



Date .....

Expt. No.....

Page No. 26

Experiment - 9

Binary to Gray code convertion

Aim: Realization of Binary to gray code converter using IC 7486

Theory; Binary Data;

The binary number system is composed of only 2 digits 0 & 1. The position of '1' and '0' in this system indicates the weights or value within the number. The weight of each successively higher position in a binary number is an increasing power of '2' (TWO).

Gray Code;

Gray code is an unweighted code which means there are no specific weights assigned to the Bit positions. The gray code exhibits only a single bit change from one code number to next. Gray code is not an Arithmatic code.

Binary to Gray code convertion;

The convertion b/w binary code & Gray code is very useful in the fields of security system, encoding etc. Using the following rules we can convert numbers from binary to Gray code.

1. The mse in the gray code is the same has corresponding digit in the binary number.

2. Going from left to right add each adjacent pair of

Teacher's Signature : _____

TRUTH TABLE:

BINARY CODE			
B_3	B_2	B_1	B_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

GRAY CODE			
G_3	G_2	G_1	G_0
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0

Date .....

Expt. No. ..... Page No. 27

binary digits to get the next Gray code digit. Do Not Consider the carrys.

Procedure;

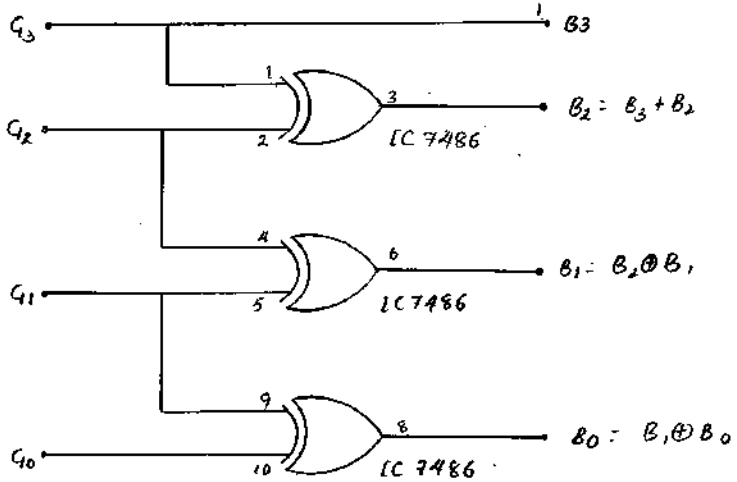
1. Insert the required good 7486 IC in ZIF socket in proper direction
2. Connect supply terminals.
3. Connect the circuits starting from the input side
4. Connect the outputs to the logic output is on the right side
5. Switch 'ON' the trainer.
6. Verify the thuth table by changing the input combinations and observe the output for each combination.
7. Write down the result

Result;

Binary code to Gray code converter has been realized using IC7486

Teacher's Signature : _____

Circuit Diagram:



Date .....

Expt. No. ..... Page No. 28

Experiment - 10

Gray Code to Binary Code conversions.

Aim: To realize Gray to Binary code conversion using IC 7486.

Binary Data:

The binary number system is composed of only 2 digits '0' & '1'. The position of '1' and '0' in this system indicate the weights or values within the number.

The weight of each successively higher position in a Binary number is an increasing power of '2' (two)

Gray Code:

Gray code is an unweighted code which means there are no specific weights assigned to the Bit positions. They gray code exhibits only a single bit change from one code number to next. Gray code is not an Arithmatic code.

Gray Code to Binary Code Conversion;

G_0, G_1, G_2, G_3 are the Gray code inputs & B_0, B_1, B_2, B_3 are the Binary outputs.

Using the following rules we can convert numbers from Gray to Binary

1. The MSB in the Binary code is in the same as corresponding digit in the gray code.
2. Add the obtained Binary digit to the gray digit in adjacent position.

Teacher's Signature : _____

TRUTH TABLE

GRAY CODE			
G_3	G_2	G_1	G_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

BINARY CODE			
B_3	B_2	B_1	B_0
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	1
0	1	1	1
0	1	0	0
0	1	0	1
1	1	1	1
1	1	1	0
1	1	0	0
1	1	0	1
1	0	0	0
1	0	0	1
1	0	1	1
1	0	1	0

Date .....

Expt. No. ..... Page No. 29

Procedure :

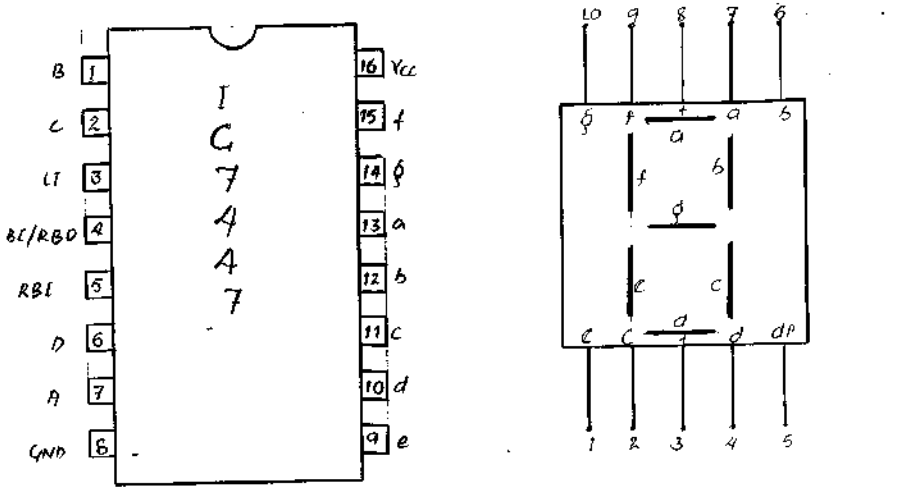
1. Insert the required good TABS IC in ZIF soket in proper direction.
2. Connect supply terminals
3. Connect the circuits starting from the inputs side
4. Connect the outputs to the logic output B_0 is on the right side.
5. Switch on the Trainer
6. Verify the truth table by changing the input combinations and observe the output for each combinations
7. Write down the result.

Result :

Gray to binary code converter has been realized using TABS.

Teacher's Signature : _____

Pin diagram:



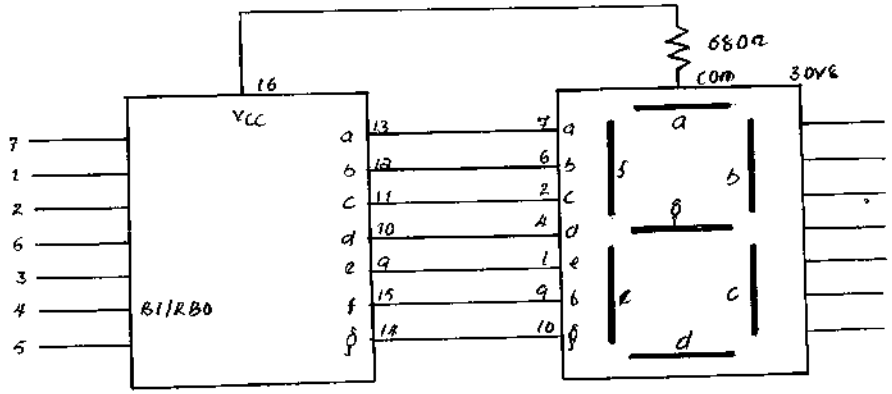
Pin details

LT ⇒ Lamp out

LT = 0 all pin of 7 Segment are HIGH

BI/RBO → Blanking I/P or ripple blanking O/P

Circuit Diagram:-



Date .....

Expt. No. ..... Page No. 30

Experiment ; 11

7 Segment Display.

Aim; Interface 7 segment display with 7447 decoder & verify the BCD to decimal conversion.

Apparatus ; Digital trainer kit.
Patch chords - 180nos
7447, Common Anode 7-segment display
680Ω Resistor

Theory ;

The visual display is more powerful & popular method for communication. The digital circuits operate on BCD signals, But it is very difficult to understand BCD signals in the form of 1's and 0's. So decoders are used to convert BCD signals into visual effect.

The 7447 is most BCD to 7-segment decoder IC which decodes or converts BCD input information into 7 segment driving signals. It generates driving signals to drive the segment display for BCD number 0 to 9. The IC 7447 is open collector decoder so it is used with common Anode display. This type of decoder are used in counters, timers, meters, watches etc.

Procedure ;

1. Insert the required IC 7447 in 16 pin ZIF socket in proper direction.
2. Insert 7-segment display in top of 40 pin socket, pin 1 of socket is 1 of display & pin 40 is in pin

Teacher's Signature : _____

LT	BI/RBO	RBI	D	C	B	A	DISPLAY	a	b	c	d	e	f	g
0	1	X	X	X	X	X	ON	H	H	H	H	H	H	H
1	0	X	X	X	X	X	OFF	L	L	L	L	L	L	L
1	1	1	0	0	0	0	0	H	H	H	H	H	H	L
1	1	1	0	0	0	1	1	L	H	H	L	L	L	L
1	1	1	0	0	1	0	2	H	H	L	H	H	L	H
1	1	1	0	0	1	1	3	H	H	H	H	L	L	H
1	1	1	0	1	0	0	4	L	H	H	L	L	H	H
1	1	1	0	1	0	1	5	H	L	H	H	L	H	H
1	1	1	0	1	1	0	6	L	L	H	H	H	H	H
1	1	1	0	1	1	1	7	H	H	H	L	L	L	H
1	1	1	1	0	0	0	8	H	H	H	H	H	H	H
1	1	1	1	0	0	1	9	H	H	H	L	L	H	H
1	1	1	0	0	0	0	BLANK	L	L	L	L	L	L	L

Date .....

Expt. No. ..... Page No. 31

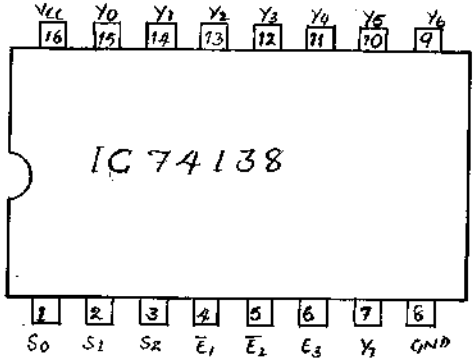
10 of display
3. Connect 680Ω register to Common Anode & Vcc on ZIF socket
4. Connect an other signals as shown in diagram & Truth table
5. Switch ON the trainer.
6. Observe the 7-segment display for different input combination as shown in truth table.
7. Write proper result.

Result;

BCD to Decimal conversion has been verified with 7447 decoder & 7-segment display.

Teacher's Signature : _____

1 1:8 DEMUX;



Pin details

S_0, S_1, S_2 = Selected i/p

E_3 = input line

$\bar{E}_1, \bar{E}_2$ = Enable i/p (Act low)

Y_0 to Y_7 = Output lines

ENABLE INPUT		I/P LINE	SELECT INPUT			OUTPUT							
$\bar{E}_1$	$\bar{E}_2$	E_3	S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
1	1	X	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Date .....

Expt. No. .....

Page No. 32

Experiment - 12.

Verification of 1:8 demux using IC 74138 & 8:1 mux using IC 74151

Aim; Verification of 1:8 demultiplexer using IC 74138 & 8:1 mux using IC 74151

Theory;

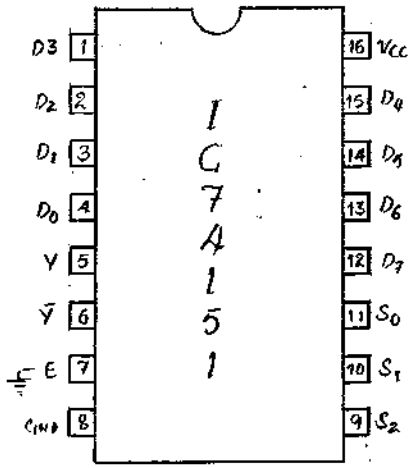
Multiplexer; It is a combinational logic circuit with many inputs & one output. We can connect any one of the input to the output by using control or select signals. It is used in digital communication at transmitter end to multiplex the many input in to using to transmit.

74151; It is MSI 8:1 multiplexer IC. It consists of 8 inputs, 1 output & control signal along with gate signals. when gate G signals is low the IC is active. D_0 to D_7 are the inputs Y is the output. The output is connected to the input dependent on the select or control signals A, B, C if CBA = 001 the Y is connected to D_1 it provides the 2 outputs Y & $\bar{Y}$.

Demultiplexer; It is a combinational logic circuit with one input & many outputs. We can connect the input to any 1 of the output by using control or select signals. It is called in digital communications. at receiver end to demultiplex the multiplexed signal with many input in to signal single to transmit with synchronize to transmitter.

Teacher's Signature : _____

PIN DIAGRAM



Pin details

D_0 to D_7 — input datalines

Y - Output lines

S_0 to S_2 — Select input

$\bar{E}$ — Enable input

TRUTH TABLE

ENABLE INPUT	SELECT INPUT			INPUT LINES								OUTPUT	
$\bar{E}$	S_2	S_1	S_0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	$\bar{Y}$
0	0	0	0	1	0	0	0	0	0	0	0	1	0
0	0	0	1	0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	1	0	0	0	0	0	1	0
0	0	1	1	0	0	0	1	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0	1	0
0	1	1	0	0	0	0	0	0	0	1	0	1	0
0	1	1	1	0	0	0	0	0	0	0	1	1	0

Date .....

Expt. No..... Page No...33.....

74138: It is a msi 1:8 demultiplexer IC. It consist 1 input + 8 outputs + control signals along with gate signals. when 2 gate (G_{2A}, G_{2B}) signal is low the IC is active. The input select or control signals A,B,C if CBA = 011 the input is connected to Y_3

Procedure:

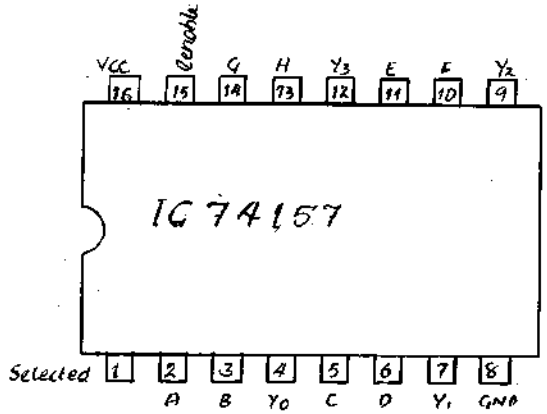
1. Connect 1:8 demultiplexer using 74138 IC
2. Connect gate signals + ABC to logic inputs.
3. Connect Y_0-Y_7 to logic outputs.
4. Keep gate signal low n select the required output.
5. Apply data at D input & observe the output.
6. check for different output lines by using select lines.
7. Connect 8:1 multiplexer using 74151 IC & verify its truth table
8. First connect the gate & select signals if no free logic inputs then connect or short to Vcc for logic 1 & GND too.
9. Write proper result.

Result:

1:8 Using IC 74138 (demux), 8:1 using IC 74151 (mux) has been verified.

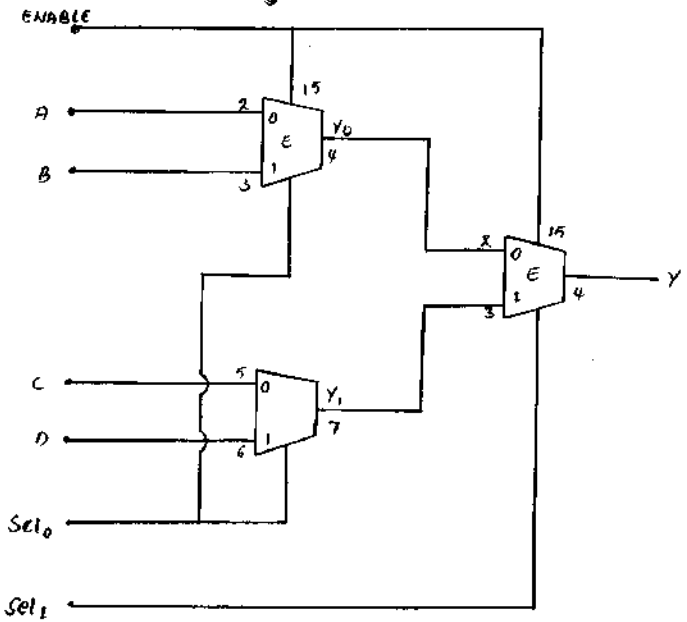
Teacher's Signature : _____

Pin Diagram:



Pin details
Select ; Select input
ABCD ; input lines
Enable ; enable input
Y ; output line

Circuit Diagram:



Date .....

Expt. No..... Page No. 34

Experiment - 13

Verification of 4:1 mux using 2:1 using IC 74157.

Aim; Verification of 4:1 mux using 2:1 using IC 74157.

Apparatus; Digital trainer kit.
Patch cards
IC 74157.

Theory; The multiplexer (or data selector) is a logic circuit that gates one out of several input to a single output. The input selected is connected by a set of select inputs for selecting one out of n i/p a set of m-i/p is required where $2^m = n$

Advantages;
1. Simplification of logic expression is not required.
2. It minimizes the IC Package count.
3. Logic design is simplified.

For using the multiplexer is a logic element, either the truth table or one of the standard forms of logic expression must be available. Normally a strobe or enable input 'E' is incorporated which helps in cascading & it is generally active low.

Procedure;
1. Connections are made has shown in figure 1 using the Pin details of IC used.

Teacher's Signature : _____

TRUTH TABLE

ENABLE	SEL 1	SEL 0	D	C	B	A	OUTPUT	
1	1	1	X	X	X	X	0	
1	0	0	X	X	X	X	0	
0	0	0	X	X	X	0	0	A
0	0	0	X	X	X	1	1	A
0	0	1	X	X	1	X	1	B
0	0	1	X	X	0	X	0	B
0	1	0	X	0	X	X	0	C
0	1	0	X	1	X	X	1	C
0	1	1	1	X	X	X	1	D
0	1	1	0	X	X	X	0	D

Date .....

Expt. No. .....

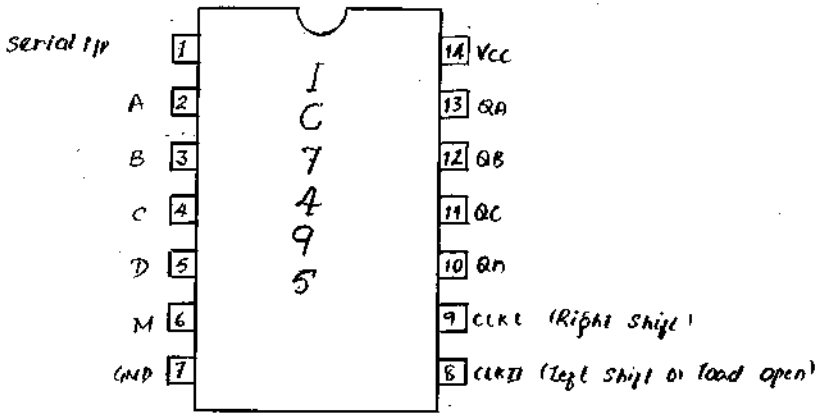
Page No. 35

2. Connect the data, select and enable input to the toggle switches and outputs to the LED's.
3. Switch on the power supply of the IC trainer.
4. for different selected input at the output as shown in the truth table.

Result:

4:1 multiplexer using 2:1 multiplexer has been verified

Teacher's Signature : _____



Pin details

Serial input ⇒ Serial data input

A,B,C,D ⇒ parallel data input

m ⇒ mode control

m = 1 ⇒ Parallel mode

Q_A, Q_B, Q_C, Q_D ⇒ Outputs

PIPO

CLK2	M	A	B	C	D	Q_A	Q_B	Q_C	Q_D
↓	1	1	0	0	1	1	0	0	1
↓	1	1	1	0	1	1	1	0	1

Date .....

Expt. No. ..... Page No. 36

Experiment - 14

Shift register using IC 7495

Aim: To construct & verify the operation of SISO, SIPO, PIPO, PISO using IC 7495.

Apparatus: Digital trainer kit
IC 7495
Patch chords.

Theory:

The IC 7495 is a 4bit shift register which allows serial in/parallel in parallel out operations as well a right shift & left shift. Thus 7495 allows all the 4 modes of the operation namely SISO, SIPO, PISO, PIPO. Apart from both right & left operation. Hence it acts as universal shift register. The IC an serial input terminals for serial data i/p parallel data can be entered through the parallel i/p's ABCD. A mode control signal identifies the serial or parallel ~~i/p's~~ mode of operation. when mode control is equal to zero the serial mode operation is performed & the parallel data is fed at Q_A, Q_B, Q_C o/p's when serial data is fed on output. The IC has a 2 CLK's CLK1 & CLK2 used for left operation & used as parallel load.

SIPO mode of Operation;

In SIPO mode of operation data bits are entered into register serially & read from the register parallely.

Teacher's Signature : _____

SISO:

CLK1	M	Serial input	Q_A	Q_B	Q_C	Q_D
0	0	0	X	X	X	X
1	0	0	0	X	X	X
2	0	1	1	0	X	X
3	0	0	0	1	0	X
4	0	1	1	0	1	0
5	0	0	0	1	0	1
6	0	0	0	0	1	0
7	0	0	0	0	0	1
8	0	0	0	0	0	0

SIPO

CLK1	M	Serial input	Q_A	Q_B	Q_C	Q_D
0	0	0	X	X	X	X
1	0	0	0	X	X	X
2	0	1	1	0	X	X
3	0	0	0	1	0	X
4	0	1	1	0	1	0

PISO:

SI	CLK2	CLK1	M	A	B	C	D	Q_A	Q_B	Q_C	Q_D
0	1	0	1	1	1	0	0	1	1	0	0
0	0	1	0	X	X	X	X	0	1	1	0
0	0	1	0	X	X	X	X	0	0	1	1
0	0	1	0	X	X	X	X	0	0	0	1
0	0	1	0	X	X	X	X	0	0	0	0

Date .....

Expt. No. .....

Page No. 31

PISO Mode of Operation:

In PISO mode of operation data bits are entered into register Parallely & read from register serialy.

PIPO:

In PIPO mode of operation data bits are entered into register parallely & read from register parallely.

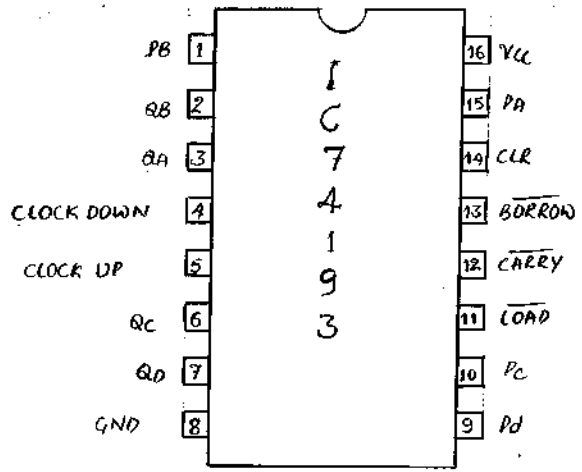
Procedure:

1. check the patch chords for continuity.
2. Insert IC 7495 in trainer kit connect Vcc & GND
3. Connect terminals for SISO operation as specified in truth table.
4. Apply data with CLK and observe specified in truth table output at last F/F QD and verify truth table.
5. Connect terminals for SIPO, PISO, PIPO & verify truth table.

Result:

Operation of shift Registers using IC 7495 is verified

Teacher's Signature : _____



Pin details

CLKUP → clock input for up count
CLK DOWN → clock input for down count
CLR → Active high clear signal
load - Active low load signal
QA - QD → Outputs
PA - PD : Parallel input.

INPUT				OUT PUT (QA - QD)
CLR	CLK UP	CLK DOWN	$\overline{LOAD}$	MODE
1	X	X	X	Reset to 0
0	↑	1	1	UP COUNT
0	1	↑	1	DOWN COUNT

Date .....

Expt. No. .....

Page No. 38

Experiment - 15

Up down counter using IC 74193.

Aim; IC 74193 [formation] familiarization & to verify truth table of up down counter.

Theory; The IC 74193 is a 4 bit binary synchronous up down counter with Asynchronous set and preset facilities. It has 2 clks, clk up & clk down selection of one of these clock determines the direction of counting operations. The IC also has active high clr input which can be used to reset the counter using the load signal.

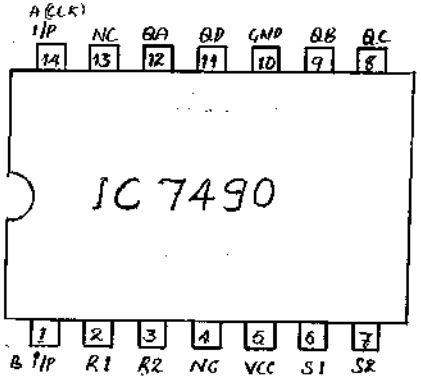
Procedure;

1. check the patch chords for continuety
2. Insert IC 74193 into Digital Trainer kit.
3. Connect Vcc & GND other connections by looking into the ic pin diagram.
4. Apply the clk pulse by refering functionle table for up/down counting
5. Apply the data input & clk also verify the truth table with proper result

Result;

IC 74193 has been familiarized and truth table of up/down counter has been verified.

Teacher's Signature : _____



Pin details

Q_A, Q_B, Q_C, Q_D = Out puts

$R_1\ R_2$ = Reset Inputs

$S_1\ S_2$ = Set inputs

When $S_1 = S_2 = 1$

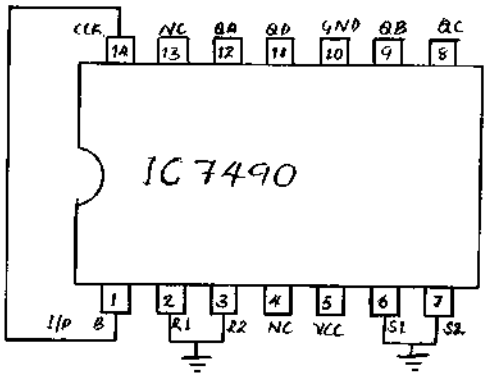
$Q_D, Q_C, Q_B\ Q_A$: 1001

For normal Counter operation

$R_1 = R_2 = 0$

$S_1 = S_2 = 0$ NC --> Not connect

Circuit Diagram



TRUTH TABLE

CLK	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

Date .....

Expt. No. .....

Page No. 39

Experiment - 16

A Synchronous Counter Using IC 7490.

Aim: To verify the truth table of Asynchronous counter & familiarization of IC 7490

Theory: The IC 7490 is an Asynchronous decade counter which consists of 4 JK master slave flip flops internally connected to provide a MOD 2 section consisting of 1 flip flop & a MOD 5 section consisting of 3 flip flops. The MOD 2 & MOD 5 section can be cascaded together to form a MOD 10 counter. The counter counts from 0000 to 1001 before it can reset. clock pulses are applied to input A (PIN-14) of 7490 IC.

Procedure:

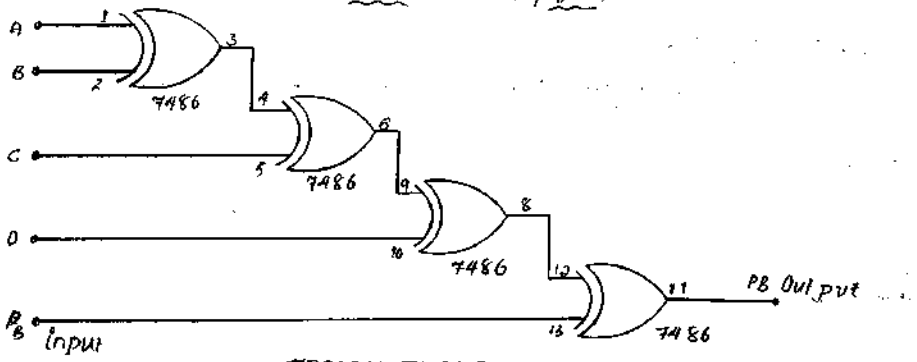
1. check the patch chords for continuety.
2. Insert the IC 7490 into Digital Trainer kit.
3. Connect Vcc & GND, make the connections has shown in the ckt.
4. Apply the data along with clk pulse & verify the truth table.
5. Write proper result.

Result:

IC 7490 has been verified and familiarized by its truth table of asynchronous counter.

Teacher's Signature : _____

CIRCUIT DIAGRAM



TRUTH TABLE

BINARY INPUT				OUTPUT	
				$P_B=1$	$P_B=0$
D	C	B	A	EVEN	ODD
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	0

Date .....

Expt. No. ..... Page No. 40

Experiment - 17.

Parity Generator

Aim: To realize parity generator & checker using IC 7486

Apparatus: Digital trainer kit.
Patch chords - 11 no's
IC - 7486

Theory:

The parity is a simple & popular method in user for error detecting & connecting method in digital communication. The parity bit indicates the number of 1's is given data. If input data consists of odd number of 1's then it is odd parity else it is even for example, a (0010) is even number but it is odd parity & a (1001) it is odd number but it is even parity. In case of 6 (0110) is even parity. The parity select signal is used to select odd or even parity output.

Procedure:

1. Connect the circuit as shown in the diagram.
2. Keep ps-0 for odd parity.
3. Verify the truth table by using changing the I/P combination & observe the output for each combination.
4. Keep ps-1 for even parity repeat step 3.
5. Write down the result.

Result: The parity generator & checker has been realized using IC 7486.

Teacher's Signature : _____

Experiment - 18

Familiarization of 4 bit & 8 bit addition Using IC 7483

Aim; Familiarization of IC 7483 with 4 bit and 8 bit addition

Apparatus; Digital trainer kit.
Patch chords - 16/32 Nos
7483 - 2 Nos

Theory;

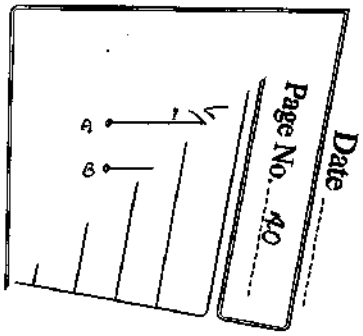
To add digits with more bit size like 4-bit or 8-bit the parallel adders are used. But ckt is complex if it is constructed by using logic gates. To simplify the task the adder ic is used. These ic's consists of 4 bit or 8 bit parallel adder. The 7483 is msi 4 bit binary parallel adder IC. It adds two 4 bits & given 5 bit output. This is 16 pin ic. It takes 2 digits A & B as inputs along with carry input & given 4-bit sum & carry as fifth bit output. more number of adder can be used to add 16/32/64 bit numbers.

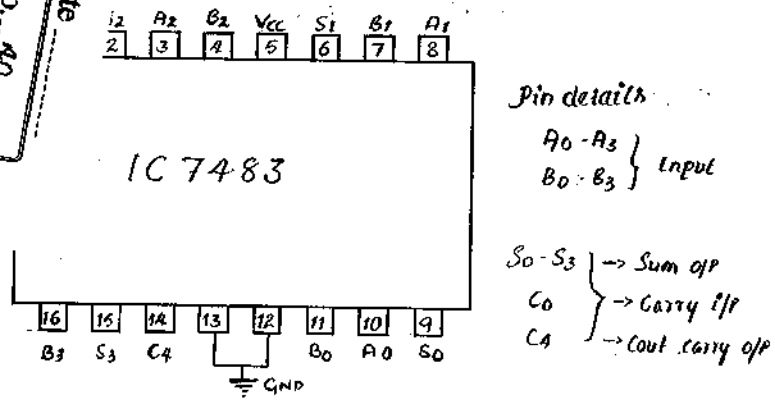
Procedure;

1. Connect the 4bit adder circuits as shown in the diagram. If inputs are not sufficient then use or short them vcc for logic '1' and GND for logic '0'

2. Verify the truth table by changing the input combinations & observe the output for each combination

Teacher's Signature : _____



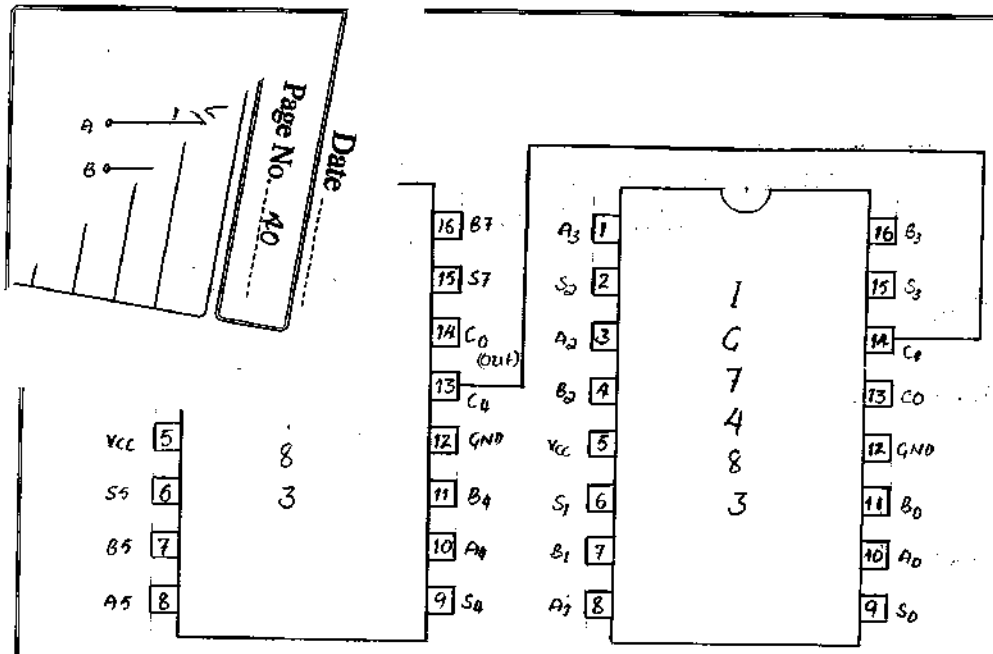


Pin details

$A_0 - A_3$, $B_0 - B_3$ } Input

$S_0 - S_3$ → Sum o/p
C_0 → Carry i/p
C_4 → Cout carry o/p

A				B				OUTPUT				
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_4	S_3	S_2	S_1	S_0
0	1	1	0	0	1	0	0	0	1	0	1	0
1	0	0	1	1	0	0	0	1	0	0	0	1
1	0	1	0	1	0	0	0	1	0	0	1	0
0	1	0	1	1	1	0	0	1	0	0	0	1



$A = A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0 = 1\ 1\ 1\ 1\ 1\ 1\ 1\ 0$

$B = B_7\ B_6\ B_5\ B_4\ B_3\ B_2\ B_1\ B_0 = 1\ 0\ 1\ 1\ 1\ 0\ 0\ 0$

$S\quad S_7\ S_6\ S_5\ S_4\ S_3\ S_2\ S_1\ S_0 : 1\ 0\ 1\ 1\ 0\ 1\ 1\ 0$

$C_{out} \qquad C_8 = 1$

$A = 10111101$

$B = 01111100$

$S = 00111001$

$C_{out} \quad 1$

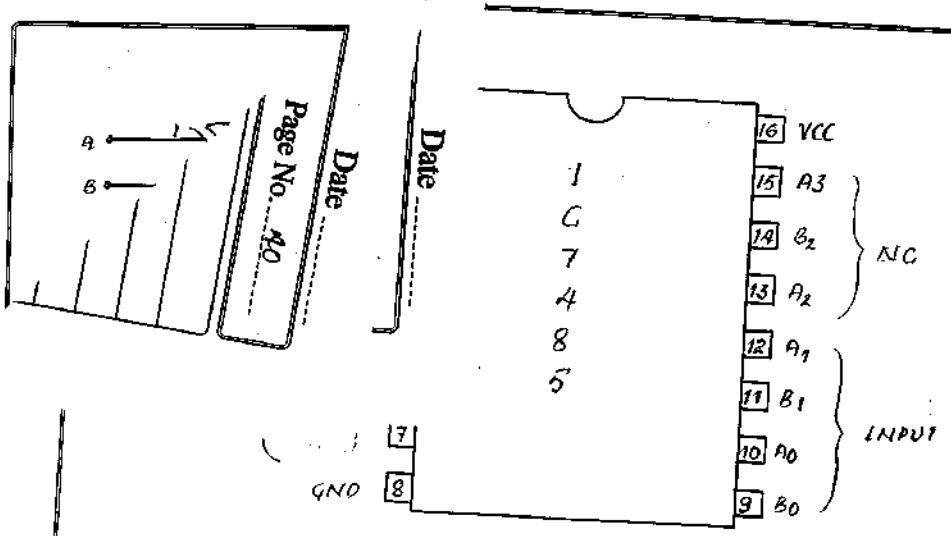
3. Connect 8 bit adder circuit as shown in diagram & verify the truth table.

4. Write proper conclusion.

Result:

IC 7483 has been familiarized & 4 bit & 8 bit addition has verified.

Teacher's Signature : _____



TRUTH TABLE

A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Date .....

Expt. No. ..... Page No. 43

Experiment - 19

2 Bit comparator.

Aim: Realization of 2 bit comparator using IC 7485

Apparatus: Digital trainer kit.
Patch chords
IC 7485 - 1 No.

Theory:

The comparator is combinational logic network which can compare two numbers and gives conditions as output.

The logic expressions for 2 bit comparator as follows.

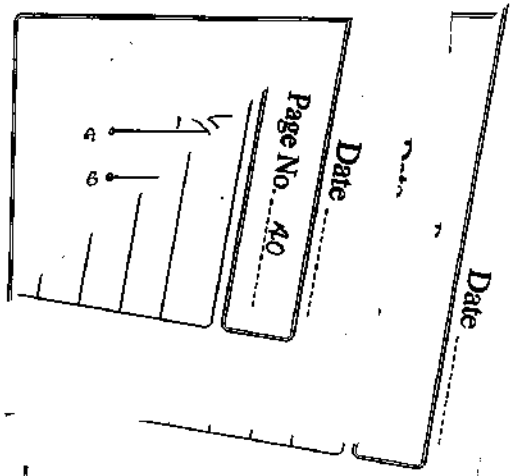
$$A=B \Rightarrow \overline{(A_0 \oplus B_0)} \cdot \overline{(A_1 \oplus B_1)}$$

$$A>B \Rightarrow (A_2(A_1+B_1)) + (A_1+B_1(A_0(A_0+B_0)))$$

$$A<B \Rightarrow (B_2(A_1+B_1)) + (A_2+B_2(B_0(A_0+B_0)))$$

When we want to compare 2 numbers with more than 2 bits circuit is complex if we use the logic gates. To over come this problem we are using IC comparators. The 7485 is a msi 4 bit comparator. It takes two 4 bit number A & B & gives its salin conditions whether A>B or A=B or A<B. The more number of 7485 comparators can be cascaded together to increase the bit size of input numbers into 8/12/20/64 bits. The cascaded inputs (A>B, A=B, A<B) are used to cascaded with other 7485 comparators. The increasing the bit size of number is useful to compare the higher magnitude numbers.

Teacher's Signature : _____



Date

Expt. No. Page No. 44

Procedure:

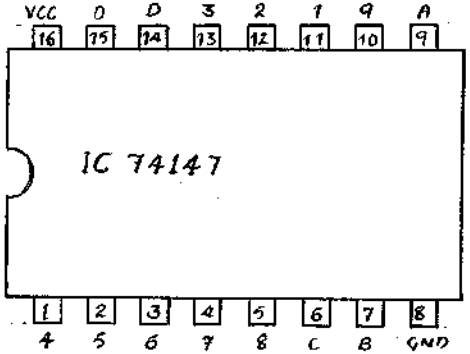
1. Connect comparator using IC 7485 & verify its truth table.
2. Verify its truth table for different input combinations.
3. Write the proper conclusion.

Result:

IC 7485 has been familiarized and a bit comparator has been realized using IC 7485.

Teacher's Signature :

PIN DIAGRAM



Pin details
0 - 9 → Input data
A - D → Output data

TRUTH TABLE

INPUT DATA LINES										BCD OUTPUT			
9	8	7	6	5	4	3	2	1	0	D	C	B	A
1	1	1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	1	0	0
1	1	1	1	1	0	1	1	1	1	1	0	1	1
1	1	1	1	0	1	1	1	1	1	1	0	1	0
1	1	1	0	1	1	1	1	1	1	1	0	0	1
1	1	0	1	1	1	1	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	0	1	1	0

Date .....

Expt. No. ..... Page No. 15

Experiment ; 20;
Verify the truth table of priority encoder using IC 74147

Aim; Verify the truth table of priority encoder using IC 74147

Apparatus; Digital trainer kit
Patch cards - 15 Nos
IC - 74147.

Theory; Encoder is a combinational logic network that converts Contrast input information into coded data. This principle is used in data compression & digital communication for example audio CD to mp3 converter, winzip etc.

74147; It is most Decimal to BCD priority encoder. It consist of 9 decimal input for 1 to 9 & 4 BCD output so 9-bit decimal input is converted into 4-bit BCD format. for example 1100 is equal to 3 to display the information outputs must inverted

Procedure;
1. Connect the encoded circuit using 74147 IC
2. Connect 0 to 9 input to logical inputs
3. Connect BCD O/P to logical O/P in order from left side D,C,B&A
4. Keep all input in high level.
5. Toggle required signal in low level & observe the output
6. Like step 5 proper verify the truth table.
7. Write proper Result.

Teacher's Signature : _____

Date .....

Expt. No.....

Page No. 46

Result:

Priority encoder has been verified using IC 74147.

Teacher's Signature : _____