0540

Code : 9EC-52

Register Number | 4 | 9 | 0 | 2 | 6 | | |

V Semester Diploma Examination, May 2012

E & C BOARD

VHDL PROGRAMMING

Time : 3 Hours] **[Max. Marks : 100**

Instructions : (1) Section – **I** is *compulsory*.

(2) Answer any **two** full questions from each of the remaining sections.

SECTION – I

1. (a) Fill in the blanks : **1 × 5 = 5**

(i) The result type for all relational operations is always the predefined type _____.

(ii) The _____ statement causes execution to jump out of the innermost loop.

(iii) The order of actuals is important in _____ association.

(iv) The operator for variable alignment is _____ in VHDL.

(v) The HDL simulator generate a library named _____ every time it compiles HDL code.

(b) Explain Entity declaration format with example. **5**

SECTION – II

2. (a) Name the primary constructs of VHDL & explain briefly. **7**

(b) Explain the different steps performed by VHDL simulator. **5**

(c) Name different styles of modelling. **3**

3. (a) Explain different classes of data objects along with declarations. **8**

(b) Explain Physical data type. Give an example. **4**

(c) Explain Process statement. **3**

4. (a) Explain different types of loop statements with examples. **6**

(b) Write entity & entity declaration for a full adder. **3**

(c) Write VHDL description of 2 × 1 Multiplexer using if – else statement. **6**

[Turn over

SECTION – III

5. (a) Explain concurrent signal alignment statement with example. 5

   (b) Explain conditional signal alignment statement with example. 5

   (c) Write data flow model of an Half adder along with logic diagram. 5

6. (a) Explain the binding between entity and architecture 5

   (b) Write logic diagram, entity and VHDL structural code of 2 × 4 Decoder with tristate output. 10

7. (a) Write switch level description of two input AND gate. 6

   (b) Write switch level description of an SR Latch 9

SECTION – IV

8. (a) Explain VHDL function, it's declaration and function call with suitable example. 8

   (b) Write VHDL code for converting unsigned integer to binary using procedure. 7

9. (a) Explain VHDL user defined type. Give example. 4

   (b) Write a note on operator overloading. 6

   (c) Explain the implementation of two dimensional array. 5

10. (a) Write a note on vailog data types. 7

    (b) Write VHDL code for finding the greatest element of an array with the help of package declaration. 8

0549

Code : 9EC-52

Register Number | | | | | | | 5 | 7 |

V Semester Diploma Examination, November 2011

E & C BOARD

VHDL PROGRAMMING

Time : 3 Hours] **[Max. Marks : 100**

Instructions : (1) Section – **I** is *compulsory*.
(2) Answer any **two** full questions from each of the remaining Sections.

SECTION – I

1. (a) Fill in the blanks : **5 × 1 = 5**
   (i) The only predefined physical data type in VHDL is _____.
   (ii) A set of signals to which the process is sensitive is defined by the _____.
   (iii) All functions must have a _____ statement with an expression.
   (iv) The operator for signal alignment is _____ in VHDL.
   (v) When the standard operator symbol is made to behave differently based on type of the operands, it is said to be _____.
   (b) Explain general format of Architecture body and list different styles of modelling. 5

SECTION – II

2. (a) Explain VHDL data types. 6
   (b) Explain the process of simulation in VHDL. 6
   (c) Define entity & write its model. 3

3. (a) What are Data objects ? How are they declared ? Explain with an example. 5
   (b) List VHDL operators. 6
   (c) Explain case statement. Give an example. 4

4. (a) Write the general form of if statement and give examples of different form. 4
   (b) Explain the general form of entity duration. Give an example. 5
   (c) Write VHDL behavioural description of D-latch using variable assignment statement. 6

[Turn over

SECTION – III

5.	(a)	Explain signal declaration and signal alignment statement with examples.	5
	(b)	Explain selected signal alignment statement, give an example.	4
	(c)	Write Data Flow model of 2 × 1 Multiplexer with active low enable (logic symbol & logic diagram also).	6
6.	(a)	Explain the binding between library and module.	7
	(b)	Write logic diagram and VHDL structural code for an SR latch with NOR gates.	8
7.	(a)	Implement switch level model of two input OR gate.	8
	(b)	Write switch level description for XNOR gate.	7

SECTION – IV

8.	(a)	Explain procedure, syntax of procedure declaration and procedure call statements with example.	8
	(b)	Write VHDL function to find the greater of two signed numbers, and call it in the main module to find the greater of two input numbers.	7
9.	(a)	Write a note on subprogram overloading.	5
	(b)	Write VHDL code for addition of two matrices with the help of package declaration.	10
10.	(a)	List different Verilog operators.	8
	(b)	Write a note on VHDL Packages.	3
	(c)	Write a note on VHDL user defined type.	4