## Paper / Subject Code: 50902 / Digital Logic Design and Analysis

## S.E. SEM - III / COMP / CHOICE BASED / NOV 2018 / 28.11.2018



Marks: 80 Marks

Duration: - 3 Hours

NB: - Question 1 is compulsory

Solve any three questions from the remaining.

1	a) Convert decimal number 576.24 into binary, base-9, octal, hexadecimal system.	04
	b) Construct hamming code for 1010 using odd parity.	04
	c) Convert (-89) <sub>10</sub> to its equivalent Sign Magnitude, 1's Complement and 2's Complement Form	04
	d) Perform (BC5) <sub>H</sub> – (A2B) <sub>H</sub> without converting to any other base	04
	e) Prove De Morgans theorem	04
2a.	Given the logic expression: $A + \overline{BC} + AB\overline{D} + ABCD$ 1. Express it in standard SOP form.	10
	2). Draw K-map and simplify.	
	3). Draw logic diagram using NOR gates only.	
2b.	Reduce using Quine McClusky method & realize the operation using only NAND gates.	10
	$F(A,B,C,D) = \prod M(0,2,3,6,7,8,9,12,13).$	
3a.	Design a 4-bit binary to gray code converter.	10
3b.	Design a 4-bit BCD adder using IC 7483 and necessary gates.	10
30.	Design a 4-bit BCD adder using IC /463 and necessary gates.	10
4a.	Implement the following logic function using all 4:1 multiplexers with the	10
	select inputs as 'B', 'C', 'D', 'E' only.	
	$F(A,B,C,D,E) = \sum m (0,1,2,3,6,8,9,10,13,15,17,20,24,30)$	
4b.	Convert a SR flip flop to J K flip flop	10
5.0	Design a mad 6 symphosocya acymten yeing T FF	10
5a.	Design a mod-6 synchronous counter using T FF	
5b.	Explain the operation of 4-bit universal shift register.	10
6	Write short notes on any two	20
a.	VHDL	
b.	TTL and CMOS logic families 4-bit Magnitude comparator	
c. d.	3 to 8 line decoder	