(10)

(10)

(3 Hours)

[Total Marks: 80]

N.B.	: (1)	Question No. 1 is Compulsory .	
	(2)	Attempt any three questions out of remaining five.	
	(3)	Each question carries 20 marks and sub-question carry equal marks.	
	(4)	Assume suitable data if required.	CONT.
1.	(a)	Convert the following numbers as mentioned against them:	(5)
		(I) (101011) ₂ convert to decimal number.	
		(II) Convert (129.625) ₁₀ Hexadecimal form.	A TON
		(III) Write (-20) ₁₀ in Two's complement form.	S OI
	(b)	Write differences between synchronous and asynchronous counters.	(5)
	(c)	Explain use of latch as a switch debouncer	(5)
	(d)	Explain current and voltage parameters of logic families.	(5)
2.	(a)	Simplify using Quine McCluskey method and draw the logic diagram using basic gates for the following function; $Y = F(A, B, C, D) = \Sigma m(5, 11, 13, 14, 15) + \Sigma d(4, 6, 7)$.	(10)
	(b)	Draw four bit Ring counter and explain its operation.	(10)
3.	(a)	Implement the following function using only one 4:1 multiplexer and gates;	(10)
	(b)	$Y=F(A,B,C,D) = \Sigma m$ (2, 3, 5, 7,10, 11, 12, 13) Design 3 bit look ahead carry generator circuit.	(10)
4.	(a)	Draw circuit diagram of 2 input TTL NAND gate and explain its operation.	(10)
	(b)	Implement full adder using decoder having active low outputs and gates with fan in 2.	(10)
5.	(a)	Design lockout free mod 10 up synchronous counter using JKMS flip flops.	(10)
500	(b)	Explain parity circuits.	(10)

Convert the flip flop (I) JKMS to D flip flop (II) SR to T flip flop.

Design 8 bit comparator using 4 bit comparator IC 7485 and explain its

(a)

(b)

operation.